Unique Applications for the LTC1062 Lowpass Filter

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The LTC1062 As A Loop Filter

With commercially available PLLs, the loop filter is designed by the user to optimize the loop performance. For a variety of applications, a 1st or 2nd order lowpass passive or active R, C filter will do the job. When minimum output jitter and good transient response are required simultaneously, the design of the loop filter becomes more sophisticated. For instance, a fast transient response implies wide filter bandwidth and a reduced VCO output jitter implies minimum ripple at the VCO input. This is achieved by high outband attenuation of the lowpass filter. The LTC1062 provides the above requirements as well as economy and cutoff frequency programmability to be used advantageously in PLL designs.

The circuit of Figure 1 illustrates the use of the LTC1062 as a loop filter. The power supplies for the circuit are a single 5V for the PLL and ±5V for the LTC1062. The CMOS PLL is a CD4046B. The LTC1062 can also be used with a single 5V with some additional level shifting (see AN20). Phase detector #2 drives a diode-resistor limiter combination to make the voltage at input R of the LTC1062 swing from one diode above ground to one diode below the 5V supply. Additionally, the two 5k resistors establish a maximum AC impedance to keep the LTC1062 in its operating region and to bias the VCO input at its mid point when phase detector #2 switches into a three-state mode.

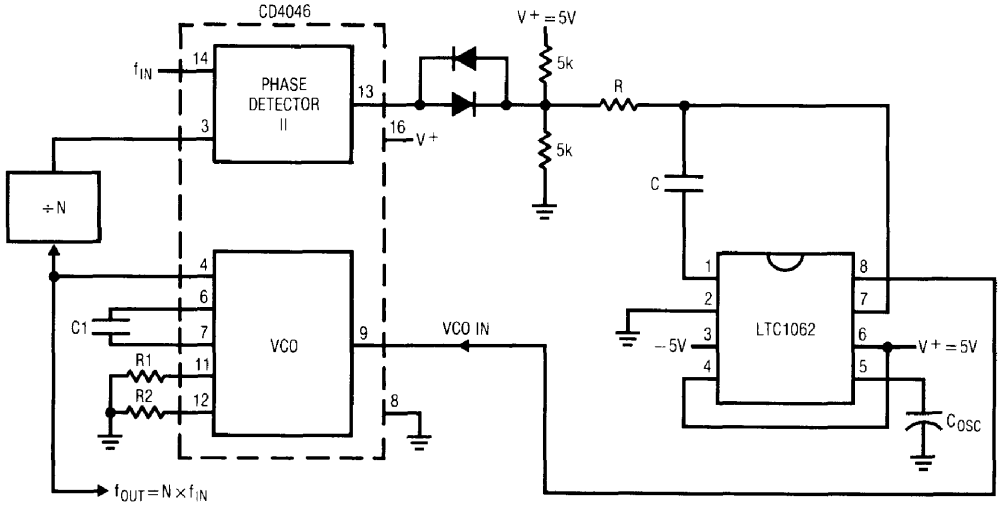


Figure 1

An empirical design procedure for input frequencies less than 5kHz ($f_{IN} \leq 5kHz$, Figure 1) is illustrated below:

- Given the minimum input frequency value, the cutoff frequency, f_C, of the LTC1062 should be chosen as:

  $1/6\,(f_{IN(MIN)}) \leq f_C \leq 1/4\,(f_{IN(MIN)})$

  The internal (or external) clock frequency of the LTC1062 should be 150 to 250 times the desired cutoff frequency, f_C.

- The capacitor C_{OSC} setting the LTC1062's internal oscillator should be chosen by:

  $$C_{OSC} = \left(\frac{130kHz}{250 \times f_C} - 1\right) \times 33pF$$

  By further decreasing the value of C_{OSC}, the internal clock frequency of the LTC1062 increases and the damping of the loop also increases.

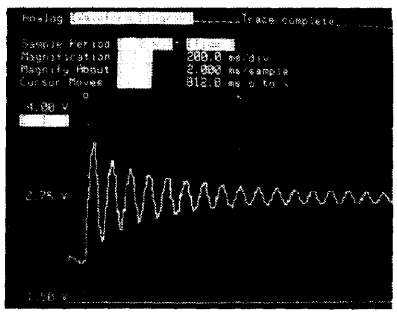
- By letting the value of $C = 0.047\mu F$, the LTC1062 input resistor R should be:

  $$R \simeq \frac{5500k\Omega}{f_C\,(Hz)}$$

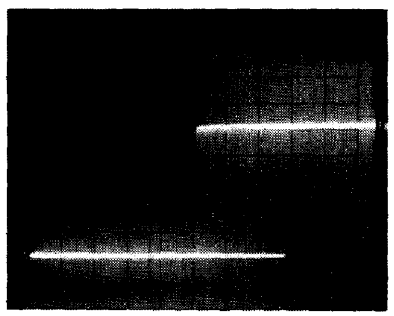
  Note: For this application, the loop filter is not required to be maximum flat and, therefore, the (R, C) values of the LTC1062 can be within ±5% tolerance.

To illustrate the performance difference between a low-pass passive R, C loop filter and the LTC1062, the circuit of Figure 1 was tested for two different PLL input frequency ranges.

The first case is a PLL with a 60Hz ±10% input frequency range and with ÷N = 100. Then, the PLL's VCO output could be used to drive the clock input of a precision switched capacitor filter, such as an LTC1060A set up in a 100:1 clock to center ratio, and configured as a 60Hz sharp notch or bandpass filter. Figure 2A shows the transient response of the loop when a passive R,C loop filter, Figure 3,

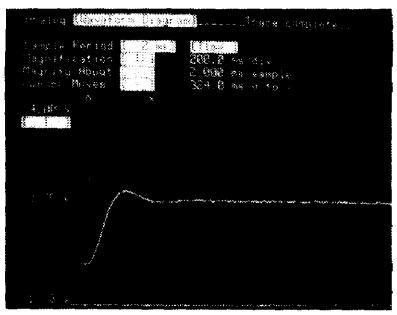


(A) 200ms

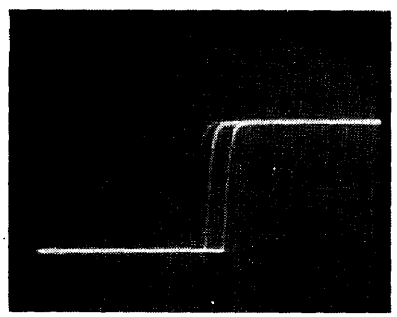


(B) 1V/DIV 10μs/DIV

Transient response (A) and jitter (B) of the PLL with a passive R, C loop filter. The output frequency of the VCO is 6kHz and the ÷N = 100.



(C) 200ms/DIV



(D) 1μs/DIV

Transient response (C) and jitter (D) of the PLL with the LTC1062 used as a loop filter. The VCO output frequency is 6kHz and the ÷N = 100. The jitter is reduced to the internal jitter of the VCO.

Figure 2

is used. The input frequency is shifted from 54Hz to 60Hz and the loop takes 820ms to settle within 5% of its steady stable value. The corner frequency of the R, C passive filter is 22Hz. The natural frequency of the loop is approximately 10Hz and the damping factor less than 0.1. Figure 2B shows the jitter at the VCO output under the above conditions. A 30μs jitter with f_{OUT} = 6kHz corresponds to 18% instantaneous frequency inaccuracy. This makes the PLL VCO output unusable as a clock generator for a tracking switched capacitor filter. A small improvement in the VCO output jitter could be achieved by further decreasing the filter's cutoff frequency; this, however, would further penalize the circuit's settling time.

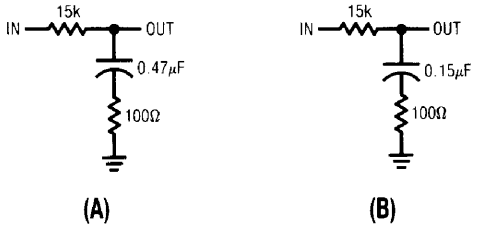
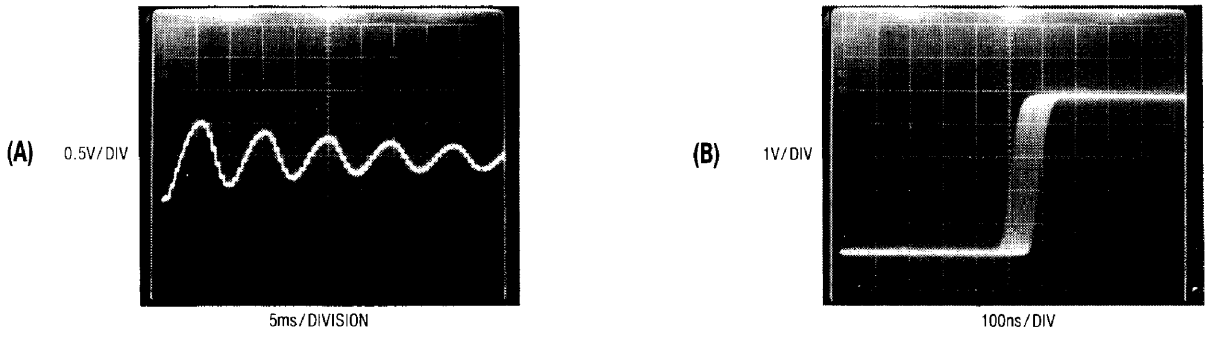


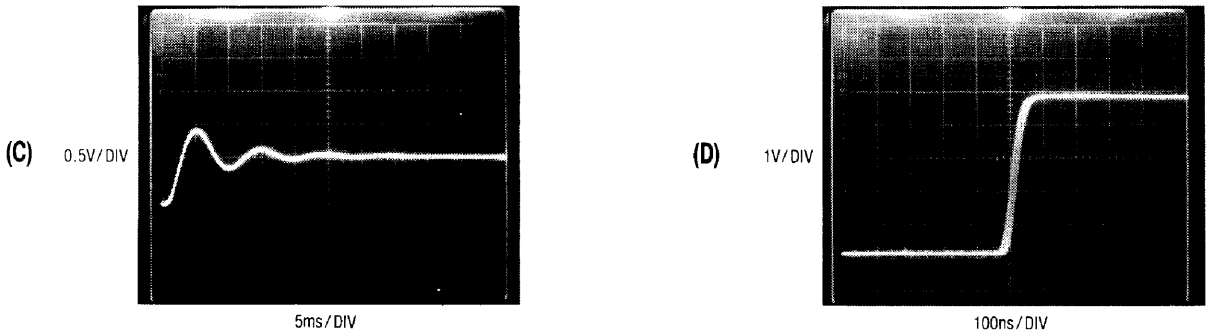
Figure 3. Lowpass R, C Filters used for the 2 PLL Examples

Figures 2C and 2D show the PLL performance when an LTC1062 is used as a loop filter. The corner frequency f_C of the LTC1062 was set at 9.5Hz ($\simeq 1/6 \cdot f_{IN}$) and its internal clock was set for 2.4kHz ($\simeq 252 \times f_C$). The settling time of the loop was 320ms and the damping factor was optimally set to 0.7. The 1μs VCO output jitter, f_{OUT} = 6kHz, was measured over 5 periods and it is attributed to the inherited jitter of the VCO internal circuitry. With the LTC1062 used as a loop filter, the circuit's jitter corresponds to 0.12% frequency error. This is quite adequate to drive the clock input of 0.3% accurate switched capacitor filters, such as LTC1059A or LTC1060A.

For the second example, the circuitry of Figure 1 was set for a PLL input of f_{IN} = 1400Hz ±30% and a divide by N = 128. The circuit's transient response, when the input shifted from 1260Hz to 1540Hz and when an R, C passive loop filter was used, is shown in Figure 4. The cutoff frequency of the R, C passive, Figure 3B, was set at 53Hz. The VCO output jitter, Figure 4B, was Δt = 90ns and was measured over 5 periods. This yields a $\Delta t/5T \times 100\% = 0.32\%$ total phase jitter of the output frequency, $f_{OUT} = 1400 \times 128 = 179.2$kHz.



Transient response (A) and jitter (B) of the PLL with a passive R, C loop filter. the output frequency is f_{OUT} = 179.2kHz and the ÷N = 128.



Transient response (C) and jitter (D) of the PLL when an LTC1062 is used as a loop filter, the output frequency, f_{OUT} = 179.2kHz and the ÷N = 128.

Figure 4

Figures 4C and 4D show the loop's performance when an LTC1062 replaces the R, C passive filter. The LTC1062 was set for a cutoff frequency of $f_C = 250Hz$ or 1/5 of the $f_{IN(MIN)}$. The internal oscillator of the LTC1062 was set at 43kHz or 172 times its cutoff frequency. The VCO output jitter was $\Delta t = 30ns$ (or 0.09%) and was measured over 6 periods. Note the excellent transient response of the circuit, Figure 4C, when compared to the underdamped response, Figure 4A.

These two PLL cases demonstrate the advantages of using the LTC1062 as a loop filter in conjunction with the CD4046B phase locked loop. For a variety of low frequency inputs and high ÷ N numbers, the LTC1062 allows the loop to simultaneously achieve good transient response and minimum output jitter. For best results, use the LTC1062 for PLL input frequencies below 5kHz and when the CD4046B operates with a single 5V supply, set 2.75V bias at the VCO input as the center of the tracking range. The minimum and maximum locking range settings of the VCO input should then be 2.25V and 3.25V, respectively.

Clock Sweepable Pseudo Bandpass/Notch Filters

If the feedback capacitor from pins 1 to 7 is replaced with a resistor, Figure 5, the circuit loses its lowpass characteristics and the response of the filter becomes selective like a bandpass. Also, since the two external components (R2, R1) are frequency independent, *the LTC1062 can be fully swept with an external clock.*

Figure 6 shows the frequency response of Figure 5, for a clock frequency of 100kHz. Figure 7 shows the variation of the peak gain, Hop, and the peak frequency, f_p, of Figure 6 versus different values of the (R1/R2) resistor ratio.

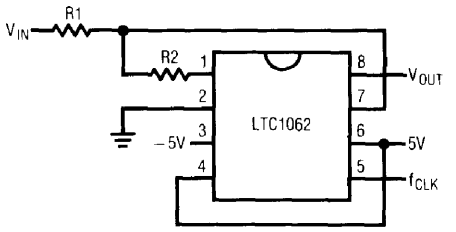


Figure 5

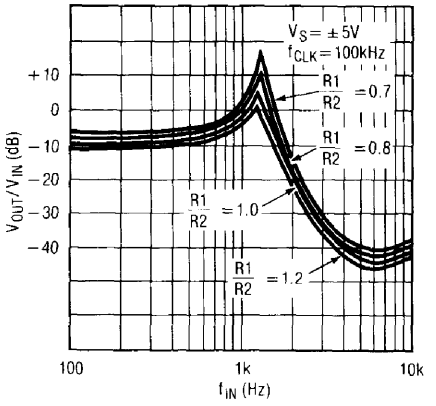


Figure 6

As can be seen from Figure 7, the resistor ratio (R1, R2) alters mainly the peak gain of the filter and has very little effect on the value of the peak frequency of Figures 5 or 6. Because of this, two LTC1062s can now be stagger-tuned with a common clock, as shown in Figures 8 and 9, to produce a respectable bandpass response.

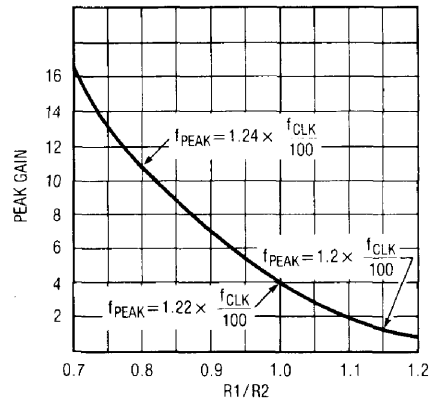
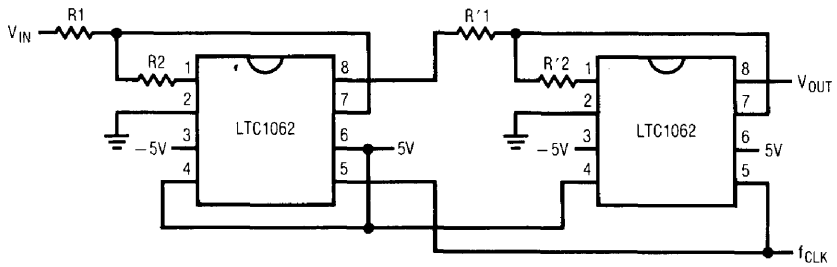


Figure 7



R1 = 10k, R2 = 10k
R'1 = 10k, R'2 = 12.5k

Figure 8. Cascading Two LTC1062s to Form a Very Selective Clock Sweepable Bandpass

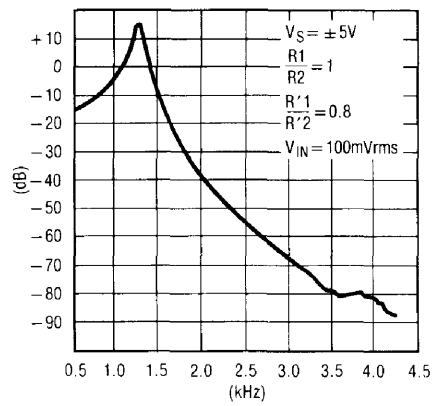


Figure 9

In Figure 6, the – 180° phase shift occurs just before the frequency of the peak. Using this property and summing the output of the bandpass filter, Figure 10, with the input voltage, a clock tunable notch response is realized, Figure 11. The clock to notch frequency ratio is 79.3:1 and it is predictable and repeatable from part to part. The notch frequency response of Figure 11 is obtained by setting the ratio (R1/R2) equal to 1.24 and by letting all the gain resistors be equal. Standard 1% value resistors will produce a 40dB deep notch. Additional notch depth can be obtained by tuning resistor R1.

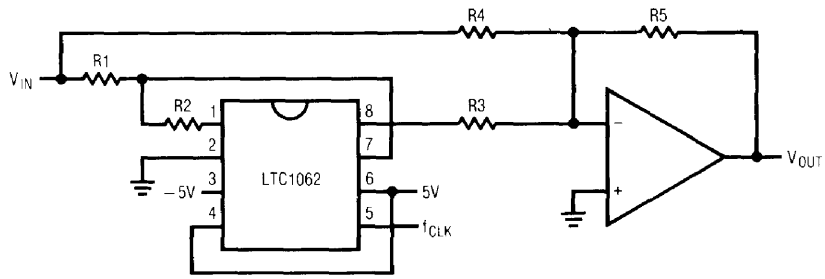


Figure 10. Clock Tunable Notch Filter
For simplicity use R3 = R4 = R5 = 10k;
$$\frac{R1}{R2} = 1.234, \frac{f_{CLK}}{f_{notch}} = \frac{79.3}{1}$$

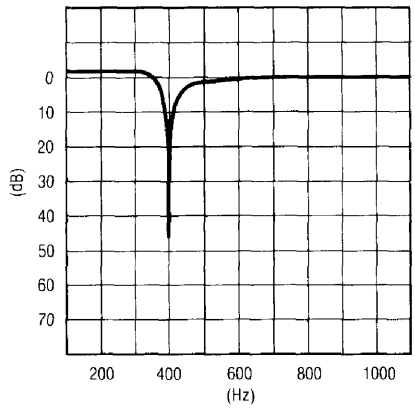


Figure 11. LTC1062 Notch Response

Accommodating High Input Voltages

High input voltages outside the input common-mode range of the LTC1062 can be divided down through a simple resistor divider, Figure 12. The DC gain of the lowpass filter is R2/(R1 + R2) and for maximum passband flatness, the paralleled combination of R1, R2 should be chosen as:

$$\frac{1}{2\pi(R1//R2)\times C} = \frac{f_{CUTOFF}}{1.63};\ R1//R2 \geq 5k\Omega$$

Note, in Figure 12, there is no need for an external op amp to buffer the divided down input voltage. The internal buffer input, pin 7, performs this function.

An obvious and often encountered application is to use this technique to interface the LTC1062 with op amps powered from ±15V supplies, Figure 13. Two inexpensive 7V zeners limit the LTC1062 power supply voltage to ±8V; meanwhile, the output of the op amp A is divided by 2. The DC accurate output of the LTC1062 is then amplified by 2. For this application, an LT1013 precision dual op amp is recommended. The maximum DC output voltage will be 300μV if the A grade of the LT1013 is used.

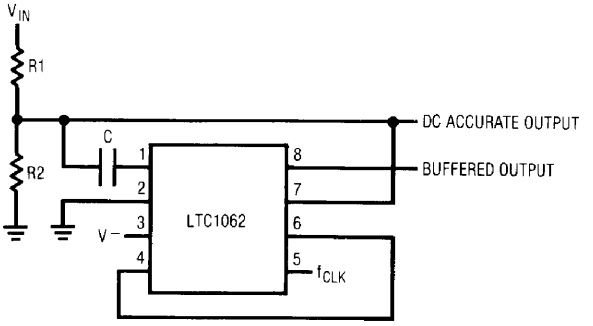


Figure 12. Using Input Resistor Divider to Accommodate High DC and/or AC Input Voltages. Pin 7 DC Buffers the Input Voltage.

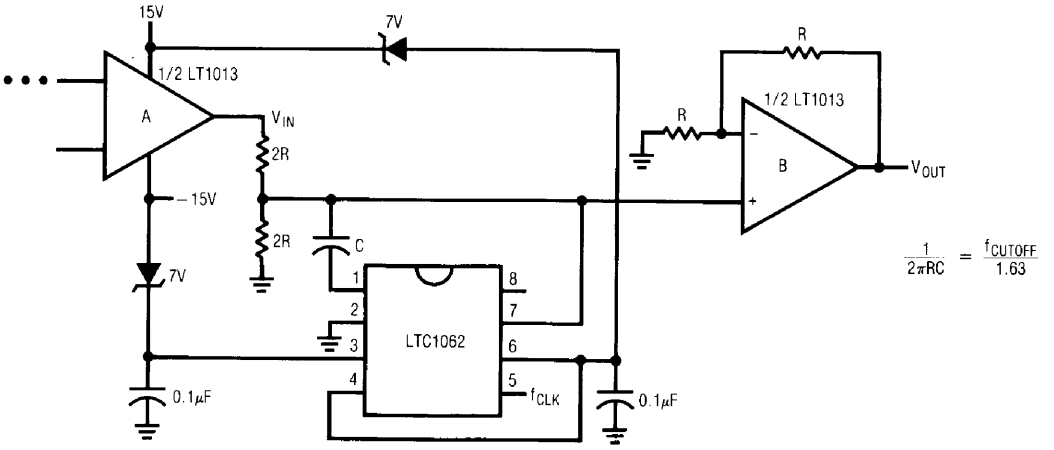


Figure 13. Using the LTC1062 in Conjunction with Precision Op Amps Operating from ±15V Power Supply

Programming Various Cutoff Frequencies

To obtain several cutoff frequencies with a single LTC1062, the clock frequency and the external R x C product should be simultaneously varied such as:

$$\frac{1}{2\pi RC} = \frac{f_C}{1.64} = \frac{f_{CLOCK}}{164}$$

For instance, to double the filter's cutoff frequency, we should double the clock frequency and, at the same time, divide by two the R x C product of the external resistor-capacitor combination. With a dual four channel multiplexer, we can easily obtain four different cutoff frequencies by selecting four input resistors and four clock frequencies. In Figure 14, the clock frequencies, all of them being ≤50kHz, where derived through a simple R, C oscillator.

Applying an External Clock Before the Power Supplies are ON

If the clock at pin 5 is externally applied before the power supplies turn ON, the device will latch. To avoid this, insert a 500Ω resistor or in series with pin 5. This will prevent latch up over temperature. If the power supplies exceed ±6V, the input protection resistor should be increased to 1k.

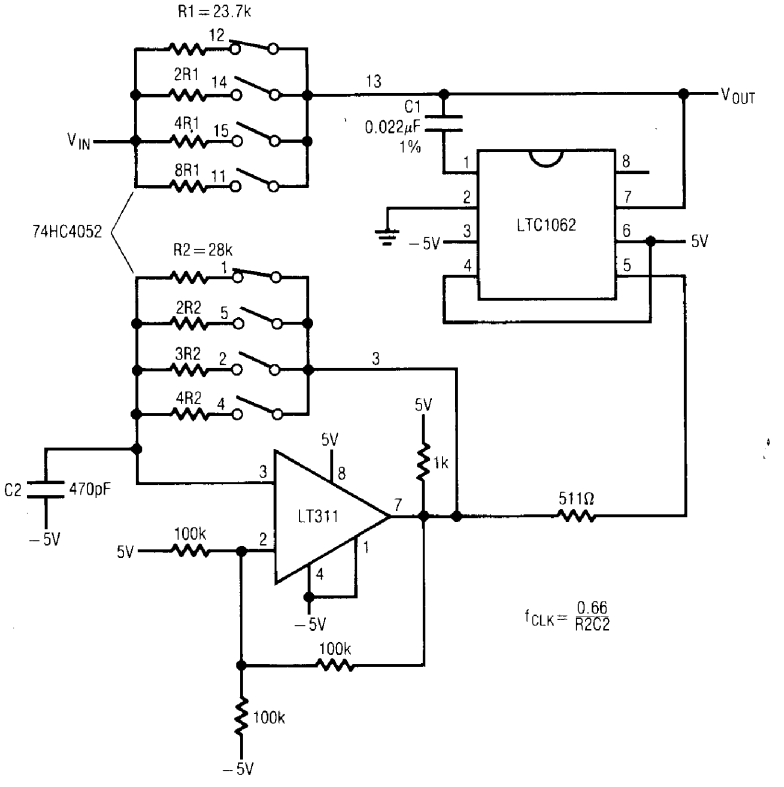


Figure 14. Using a Dual 4-Channel Multiplexer to Obtain Four Different Cutoff Frequencies (500Hz, 250Hz, 125Hz, 62.5Hz).